REPORT DOCUMENTATION PAGE

Form Approved
OMB No. 0704-0188

PLEASE DO NOT RETURN YOUR FORM TO THE ABOVE ADDRESS.

1. REPORT DATE *(DD-MM-YYYY)*	2. REPORT TYPE	3. DATES COVERED *(From - To)*
11/24/10	Final	9/24/09 to 11/24/10

4. TITLE AND SUBTITLE

Industrial Based Innovation Fund (IBIF) BAA 0003-09

Industrial Base Innovation Fund – Integrated Circuit Emulation Manufacturing Design Capability Improvements

5a. CONTRACT NUMBER

SP4701-09-C-0018

5b. GRANT NUMBER

5c. PROGRAM ELEMENT NUMBER

6. AUTHOR(S)

Mr. Milton Diaz
Group Leader
Sarnoff Corporation

5d. PROJECT NUMBER

5e. TASK NUMBER

5f. WORK UNIT NUMBER

7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)

Sarnoff Corporation
201 Washington Road
Princeton, NJ 08540

8. PERFORMING ORGANIZATION REPORT NUMBER

WBS# 13101

9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)

Defense Supply Center Philadelphia
700 Robbins Avenue, Bldg. 26-1
Philadelphia, PA 19111-5096
John Dormer 215-737-2284
john.dormer@dla.mil

10. SPONSOR/MONITOR'S ACRONYM(S)

IBIF

11. SPONSOR/MONITOR'S REPORT NUMBER(S)

12. DISTRIBUTION/AVAILABILITY STATEMENT

Approved for public release; distribution is unlimited.

13. SUPPLEMENTARY NOTES

14. ABSTRACT

Lack of availability of Integrated Circuits (ICs) continues to have an adverse impact on the readiness of military systems, and is a significant cost-driver for DoD. The Defense Logistics Agency (DLA) has two successful IC manufacturing (microcircuit emulation) programs, which address these issues. The ability to accurately and cost effectively design emulated microcircuits, is a fundamental prerequisite to ensure the successful manufacturing of the Form, Fit, Function and Interface (F3I) ICs required by DLA to support military weapon systems. Manufacturing technology improvements to the emulation design capability to significantly reduce design cycle-time by as much as 50%, significantly increase the ability to address more complex modern ICs by 17X, and provide the isolated design environment required to support a Trusted environment have been implemented into the emulation manufacturing flow. The benefits to the military supply chains are less pressure for life-time buys, reduction in lead-time for spare parts and a long-term source of supply for a larger number of NSNs.

15. SUBJECT TERMS

microcircuit emulation, microcircuit design, trust in integrated circuits, integrated circuit design, integrated circuit emulation

16. SECURITY CLASSIFICATION OF:			17. LIMITATION OF ABSTRACT	18. NUMBER OF PAGES	19a. NAME OF RESPONSIBLE PERSON
a. REPORT	b. ABSTRACT	c. THIS PAGE			Mr. Milton Diaz
U	U	UU	UU	27	19b. TELEPHONE NUMBER *(Include area code)* 609-734-2769

IBIF

Integrated Circuit Emulation Manufacturing Design Capability Improvements

Final Technical Report

October 24th, 2009 to November 24th, 2010

Contract No. SP4701-09-C-0018

Submitted November 23rd, 2010

Program Manager:

Milton Diaz

Group Leader – IC Design

Tel. #: 609-734-2769

e-mail: mdiaz@sarnoff.com

Contents

Section I

Introduction

The Department of Defense's (DoD) low-volume demand for Integrated Circuits (ICs), the constantly decreasing IC supplier base, the continual shortening of commercial IC product life-cycles, and the rise of counterfeit ICs in the supply chain are just a few of the challenges the Defense Logistics Agency (DLA) faces when addressing Warfighter microelectronics requirements. Lack of availability of ICs continues to have an adverse impact on the readiness of military systems, and is a significant cost-driver for DoD. DLA has two successful IC manufacturing (microcircuit emulation) programs, which address these issues. To date, these programs have supplied over 100,000 microcircuits in support of over 375 unique weapons systems applications including F-15, F/A-18, F-22, C-17, AEGIS, Phalanx, and the Bradley Fighting Vehicle. The emulation programs have saved the Government over $700 million in costly redesign efforts. One of the fundamental steps in the emulation manufacturing process is the accurate and cost effective design of a F3I drop in replacement for an obsolete microcircuit that meets all of the specifications of the original microcircuit. Manufacturing technology improvements to the emulation design capability to significantly reduce design cycle-time by as much as 50%, significantly increase the ability to address more complex modern ICs by 17X, and provide the isolated design environment required to support a Trusted environment have been implemented into DLA's emulation manufacturing process flow. The benefits to the military supply chains are: less pressure for life-time buys, a long-term source of supply for a larger number of NSNs, reduction in lead-time for spare parts, and the capability to upgrade the system to design in a Trusted environment.

Design Process

ICs are three-dimensional, multilayer structures, constructed layer-by-layer. Transistors are built within the silicon base layers; these are subsequently connected together to build logic functions or gates. Depending on the complexity of the IC, varying numbers of metallic wiring layers are required to provide connections between the logic functions. Accurate IC design requires modeling the many electrical and physical elements of the IC. Wafer foundry-specific information is used to accurately describe all of these interactions in a circuit model. This model assures the correct functionality of the IC in its system environment and platform.

The design of emulated microcircuits can be divided into two phases: logical or front-end; and physical or back-end. At the front end of the design process, circuits are simulated to predict their electrical performance and functionality. Once this is completed, the back end design, involves the translation of the logic and circuit configurations into geometric structures. The physical interaction of the geometric layout with logic and circuit configuration is evaluated to ensure that the resulting microcircuit achieves desired function and performance. The geometric

structures are used to create the photo masks (tooling) for fabrication of semiconductor wafers used to produce emulated microcircuits. Figure 1.1 illustrates the design flow.

Each of the steps in the design process are dependent on advanced computer tools to accurately model the physical, electrical and functional characteristics of the IC. The complexities of this task lead the microcircuit industry to be one of the first to fully embrace the use of Computer Aided Design (CAD) tools. In past decades, the dramatic advances in microcircuit technology, from simple ICs to complex ASICs, have been enabled by continuing evolution and advancement of computer systems and CAD tools. Computer systems have advanced in computational power from improvements in processor speed, memory size, and architecture. CAD tools have evolved to take advantage of the available computer technology, adding new capabilities required for successful design in advanced technologies. In addition, improved efficiency has been achieved by automating previously manual functions.

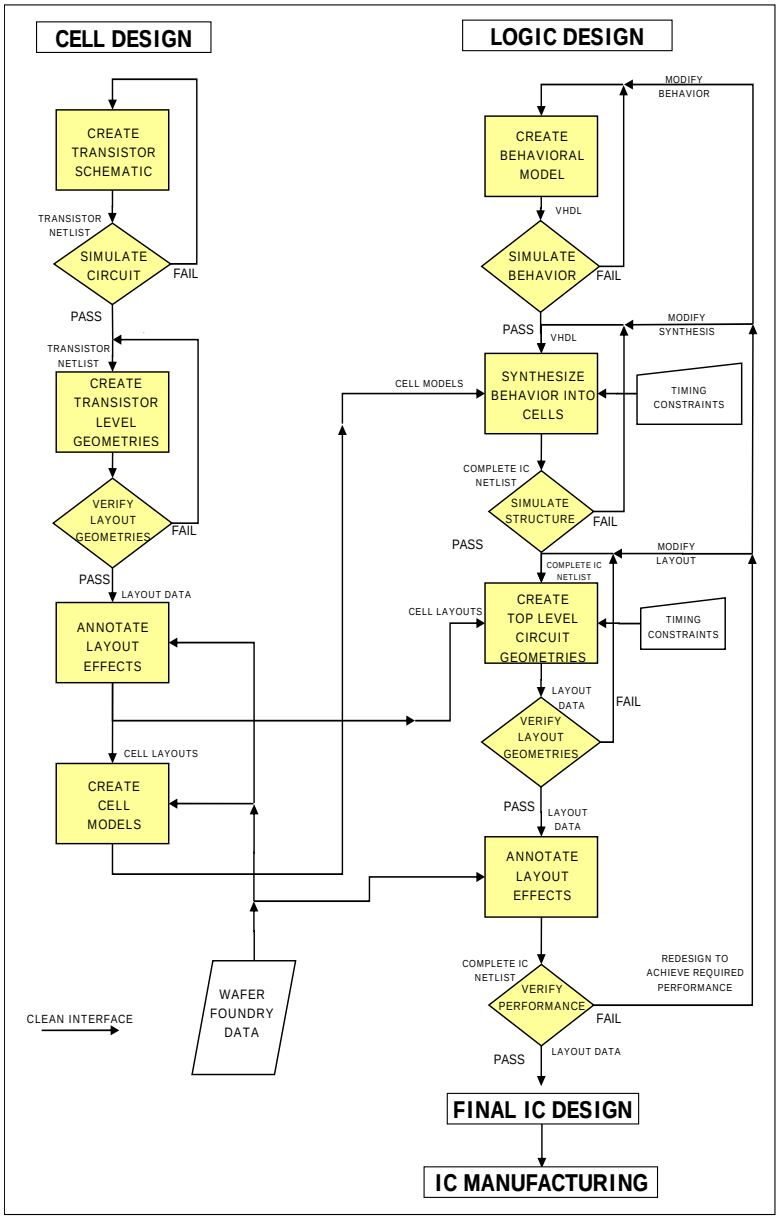


Figure 1.1 - Design Flow

Summary

To support DLA's diverse and expanding microcircuit emulation requirements in a timely manner, the emulation design system was enhanced to a more robust, and supportable design system that allows for the integration of all of the tools required. This provides the improved performance to not only maintain the existing emulation design database, but also to address DLA's demand for the design and emulation of more complex IC's. In addition, the improved design system provides the flexibility and expandability to support both normal and surge demands.

Installation of an improved physical infrastructure:

A design system with upgraded CAD tools running on more powerful computer platforms was installed. The platforms have an Operational System (OS) that takes full advantage of the computer architecture and processors. By choosing the appropriate set of CAD tools, only one type of computer platform is required. This allows for easy maintenance and expansion of the system. In addition the use of one platform and OS substantially reduces design simulation cycle time.

The primary network server is based on a Linux platform that is known for having good stability and performance with the widely used Red Hat Linux OS. This server functions as the design database server for legacy and future emulation designs while providing full access to all CAD tool licensing software. Several Linux-based workstations, supporting front-end and back-end design tasks, were connected to the server through a multiple-port network switch. Each workstation is configured to handle Central Processing Unit (CPU) intensive simulations and graphical-intensive routines. In addition, they have identical configurations capable of handling all requirements needed for each step in the design process. This allows any user to perform their assigned task on any workstation in the network. Uninterruptible Power Supplies (UPS's) are connected to all workstations and the main server to provide continuous power and allow proper saving and shutting down of all physical devices in the event of power failure.

Back-up hardware was installed to safeguard generated design information. In times of additional computer power needs, additional mirror workstations can be easily installed. This system is completely isolated from Sarnoff's LAN and the Internet to prevent tampering of design database.

Implementation of an improved CAD suite:

The improved CAD suite of tools was installed into the hardware infrastructure. The CAD suite offers all the elements the emulation design flow requires, and guarantees seamless integration of all its tools from silicon process simulation through IC design to layout and mask data generation. The time previously required for tool-to-tool interface is completely eliminated.

The CAD tools are integrated so that interface among the various stages of design is clean and efficient, not requiring additional effort for translation. Active vendor support of these tools provides regular updates to correct and enhance particular software routines. The CAD suite is flexible to accommodate Sarnoff's wafer foundry-specific information required for the accuracy of the models developed in the design flow. The CAD tools include a multi-CPU feature that takes advantage of modern computer power to initiate long run-time simulations in an environment that does not interfere with the daily operations performed by designers on each workstation. The CAD suite provides built-in proven algorithms that fully analyze simulation results, and provide best and worst case estimates, providing an approximate forecast of fabrication yields. This flexibility aids in the preservation of a legacy design database by easily providing alternatives for migration from an obsolete design infrastructure.

A significant advantage of the improved CAD suite is the implementation of an innovative token-based licensing scheme which provides a cost-effective and flexible method to meet peak demands. Licenses are legal authorizations that allow a user to run a specific software tool on a specific machine or network for a pre-defined length of time. CAD vendors traditionally offer multi-year license agreements in which the price of one license for one tool is negotiated and agreed upon. This license often limits use of one user to one tool. With Silvaco's unique license, a pool of tokens were purchased for a fixed annual fee per token. Tokens can be used with any tool in the CAD suite and are released to the generic pool when a user completes a task and closes the tool. This effectively allows multiple users to use multiple tools under a single license agreement. This scheme also addresses surge requirements by temporarily increasing the token count with additional tokens purchased for a shorter time period.

Qualification of improved design flow:

A design flow methodology was developed that adheres to Class-Q microcircuit requirements and provides consistency when designing ICs across a wide range of technologies supported in the emulation flow. Personnel were trained on each of the tools in the CAD suite and the design flow was optimized to take full advantage of all the new features. Sarnoff's foundry-specific information was implemented into the design system to allow the use of emulation technologies. A sample of IC designs was selected to exercise each of the front-end and back-end design steps. The benefits of the physical resources with the installed CAD tool suite was measured and reported against the metrics already established. Qualification of the new design flow was performed to ensure the new integrated design system conforms to the requirements of Sarnoff's Quality Procedures, ISO-9000, and QML production standards per MIL-PRF-38535 and MIL-STD-883.

Conclusions and their condensed technical substantiations:

Manufacturing technology improvements to the emulation design capability have significantly reduced design cycle-time by more than 50%, with an average design reduction from 7 to 3 months. In addition, the improvements increase the ability to address more complex modern ICs by 17X augmenting capability for 30,000 to 500,000 gates, and provide the isolated design environment required to support a Trusted environment. These overall benefits significantly assist the ability of DLA's emulation programs to support any effort for critical ICs necessary to supply and support Warfighter equipment. The program conclusions and their technical substantiations can be seen in Table 1.1.

	Relation to Performance of Goals		
Tasks	**IC Complexity (Number of Gates)**	**Design Cycle Time**	**Accuracy Simulation vs. Measured**
Installation of improved physical infrastructure	Hardware performance allows for efficient use of resources (memory and processor) for large design databases	Single Operational System for all design tools avoids file manipulation across different systems. System is expandable for large volume of designs	-
Physical Components Installation			
Configuration of closed system			
Implementation of improved CAD suite	Design tools are equipped to handle large design simulation and verification routines. Efficient capability for visual rendering and manipulation of large layout databases.	Single CAD tool vendor provides efficient transferring of design files among tools without translation overhead	Analysis tools provide additional design performance metrics to achieve first spin success
Silvaco CAD design & layout tools			
CAD token pool installation			
Backup and redundancy management			
Qualification of improved design flow	Efficient design flow to maximize utilization of features for large design databases. Controls are installed to guarantee repeatability.	Controlled and proven design flow expedites manipulation of design database across all stages	Improved characterized library database and efficient use in system accounts for process parasitic affecting performance
User training of new design infrastructure			
Design methodology creation			
Optimization of CAD tools for emulation			
Qualification controls			
Final Results and Conclusions	17X	2.3X	1.5X
	30,000 to 500,000 gates	7 to 3 months	20% to 13%
Military Value	Reduce necessity for life-of-type buys Reduce lead-time for spare parts Reduced stem maintenance cost Long-term source of supply for a larger number of NSNs Capability to perform designs in a Trusted environment		

Table 1.1

Section II

2a. Installation of improved physical infrastructure

A robust design system with a single Operational System (OS) that can support all of the design CAD tools has been investigated. The system is composed of many elements, each providing an essential function to the overall performance in a design environment.
The acquired system is composed of the following hardware items:

- 1 Primary server PowerEdge 2950 III (Nest 1)
- 1 Secondary server PowerEdge 2950 III (Nest 2)
- 2 Smart UPS 2200VA, 120V (Server power supply backups)
- 1 Powervault 124T Autoloader (Tape Backup)
- 9 Dell T5500 Workstations (Eagle 1 thru 9)
- 9 UPS 1500VA, 120V (Workstation power supply backups)
- 2 Dell 3008FP 30" Widescreen (High Performance displays for Layout tasks)
- 1 HP LaserJet 5550dtn printer

The primary and secondary servers are the core of the infrastructure by providing data storage, allocation, manipulation and management of all services required in the execution of design tasks. These servers are optimized for the requirements of the design environment and customizable for any future needs. They contain six 1TB hard drives to store the design database, CAD tool software, licenses and are backed up by a programmable tape backup unit. These hard drives were configured in a Raid 5 array with a 6^{th} drive used as a hot-spare for additional redundancy. This configuration prevents the loss of data in case of failure from any drive. The secondary server functions as a backup or failover system for the services on the network. These servers have 32GB of memory and dual X5560 Xeon processors at 2.8GHz, 8M Cache memory each. This allows the servers to greatly enhance their performance for data management and services to all user workstations. Figure 2.1 shows the servers for the infrastructure.

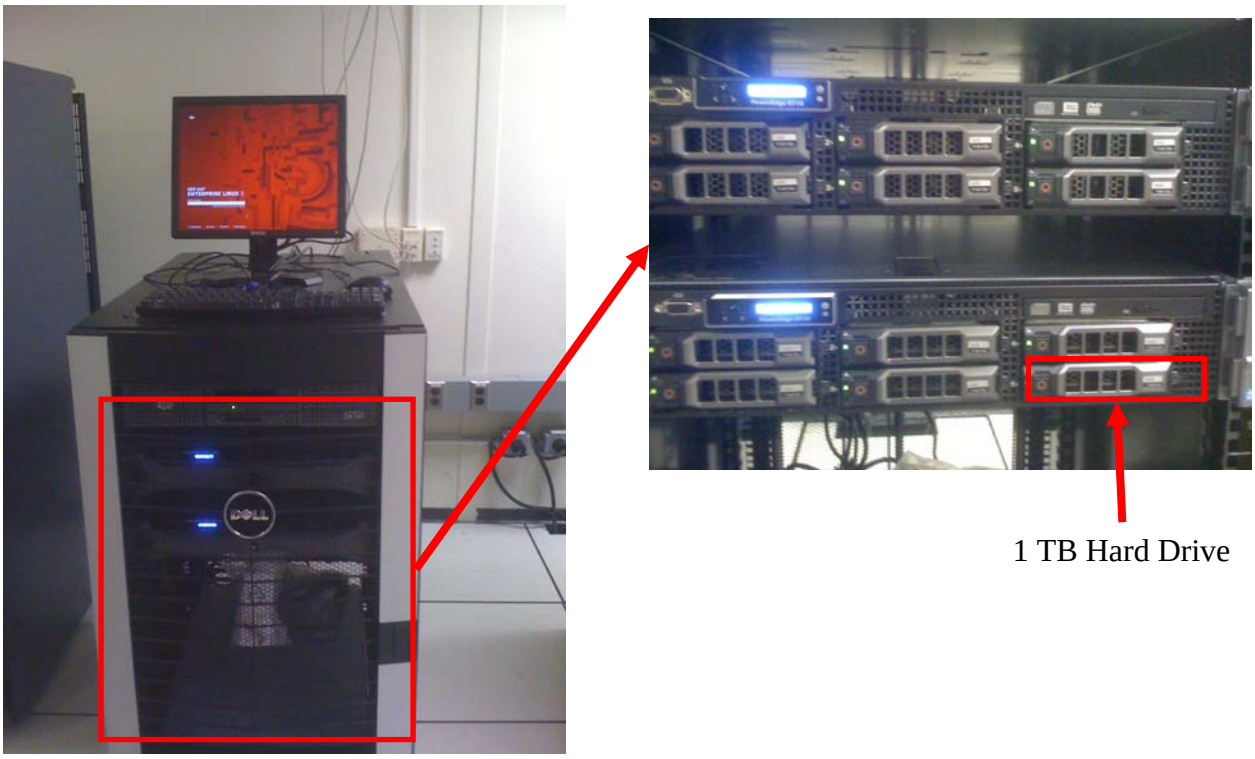


Figure 2.1 – Servers for infrastructure

Nine individual and identical workstations are configured with mirrored disks in a Raid 1 layout to also prevent loss of data. Each workstation acts as an interface to the network with simulation and processing tasks running locally. In the case of a workstation failure, a replacement can be easily configured and installed with minimal impact to the user or the system. The workstations are connected to the servers through a Virtual Local Access Network (VLAN) providing seamless interaction. The VLAN is physically isolated at the port and switch level from any public or company internal networks. The information generated by the network users is protected from any possible infiltration. Interaction with any outside systems is controlled by transferring data through hard media such as flash memory or other. This is only necessary to release layout databases to an outside mask manufacturer. The workstations have 24GB SDRAM memory, Quad Core processors X5560 with 2.8GHz speed, 8M cache memory each. These features allow each workstation to run processor intensive simulations.

All servers and workstations are also protected with Uninterruptable Power Supplies (UPS) large enough to manage the hardware load on the network. The UPS's allow approximately 10 minutes or more of power time, which is long enough to close all local and network services for a smooth shut down if necessary.

Two high performance displays were installed to allow the proper magnification and resolution required in the architecture of very dense layout databases. A LaserJet printer was added for the review of data during the design cycle. Figure 2.2 shows the overall system setup.

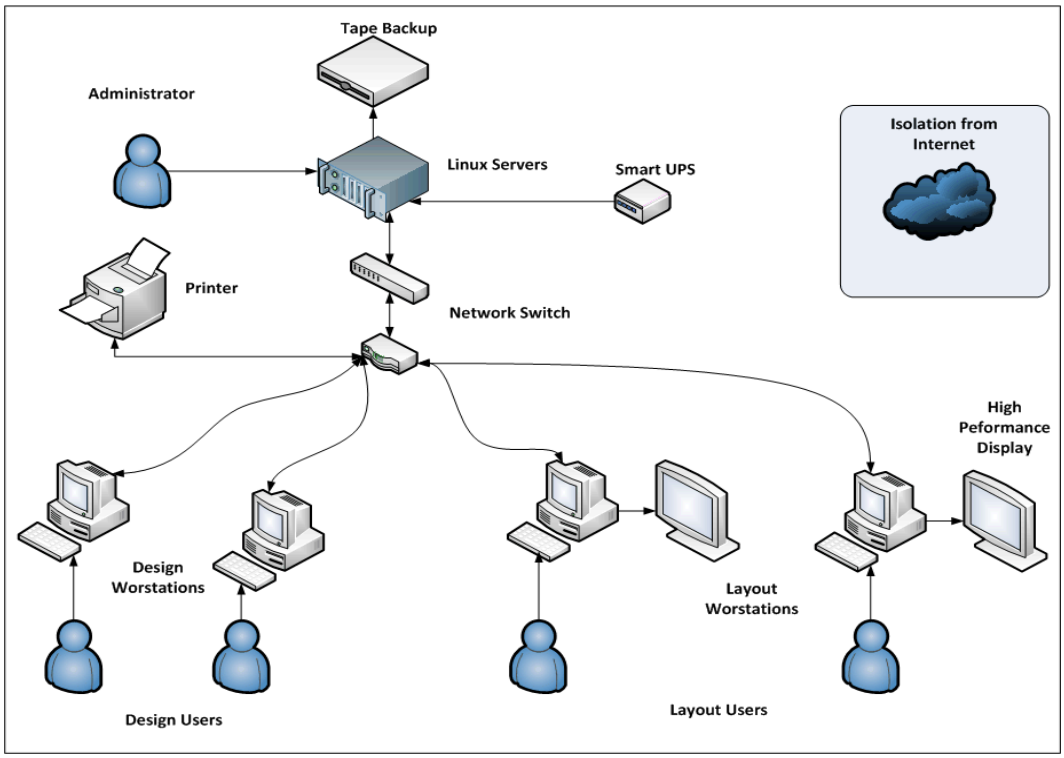


Figure 2.2 – Overall system setup

The OS and administration software (excluding design CAD) tools acquired to run on this network are:

- Red Hat Enterprise Linux 5 (Main Operation System)
- VMWare Virtual Desktop Software
- Microsoft Windows XP (Virtual OS running on VMWare)
- Double Take Backup Software
- Legato Networker
- Customized administration & startup routines provided by Silvaco.

The Red Hat Enterprise Linux environment can efficiently handle computer architectures to maximize performance. It is the main Operation System (OS) for this infrastructure running all administration and design related tools. The Virtual desktop software provides a vehicle to run an alternate "guest" operating system to add flexibility to the infrastructure and allow access to legacy tools that complement the overall design system.

The Double-Take backup software provides programmable controls to automate the replication of data from one server to the other. This replication is provided in real-time allowing short term recovery if one of the servers has a catastrophic failure.

The Legato Networker software is used to do file-based backups onto tape drives. This software is programmable to run incremental backups daily and full system backup weekly. The tape backups provide both long and short term storage of information.

In addition, Silvaco created customized administration routines for this system to easily configure additional workstations automatically and rebuild servers in case of failure. They setup the different administration services required for the system such as NIS, NFS and DNS. The system administrator is in charge of using these services for the proper management of user, group accounts, managing file systems, updating or installing applications and setting up additional security services.

Results

Each user in the system was assigned an independent account for access. The user identification is an account created for each user and administrator in the system. The User Identification Number (UID) allows the tracking of files created in the system and sets file permissions. The Group Identification Number (GID) sets the permissions for overall manipulation and creation of system files. Only administrators can modify system critical routines which are semi-transparent to the users.

The user, group configurations created and installed for the system are shown in Table 2.1

CLASS	USERID	UID	GID	NAME	
User	aschlier	220	205	Allan	Schlier
	jappelt	225	205	Janet	Appelt
	jarmer	2161	205	John	Armer
	mdiaz	8585	205	Milton	Diaz
	pjozwiak	6668	205	Phillip	Jozwiak
	safinogenov	11103	205	Semion	Afinogenov
	ggu	8965	205	Gong	Gu
Admin	dcorliss	1000	1000	Doug	Corliss
	rbenvenuto	1001	1000	Ron	Benvenuto
	tcavano	6374	1000	Ted	Cavano
	twood	1002	1000	Tom	Wood

Table 2.1

The legacy system utilized for the design infrastructure lacked the ability to be isolated and required the use of different Operational system platforms residing in different machines. Its physical size is large and maintenance is low or non-existing. Replacement for legacy hardware components is no longer available. The new system, given the name Eaglenet, has a much smaller footprint and is easily expandable. Maintenance is readily available and components are easy to obtain. The physical size of the server is only a small fraction of the original legacy servers. Figure 2.3 shows the difference among these two systems.

(a) (b)

Figure 2.3 – Comparison of (a) legacy SUN system and (b) new Linux system

This system also allows for Windows XP tools to be run in virtual form on the Linux platform. The overall advantage of this configuration is that Windows software tools take full advantage of the class performance of the new infrastructure. Also, the design structure residing on the Linux environment is accessible from the Virtual OS. Figure 2.4 shows how the virtual environment is observed from the Linux OS.

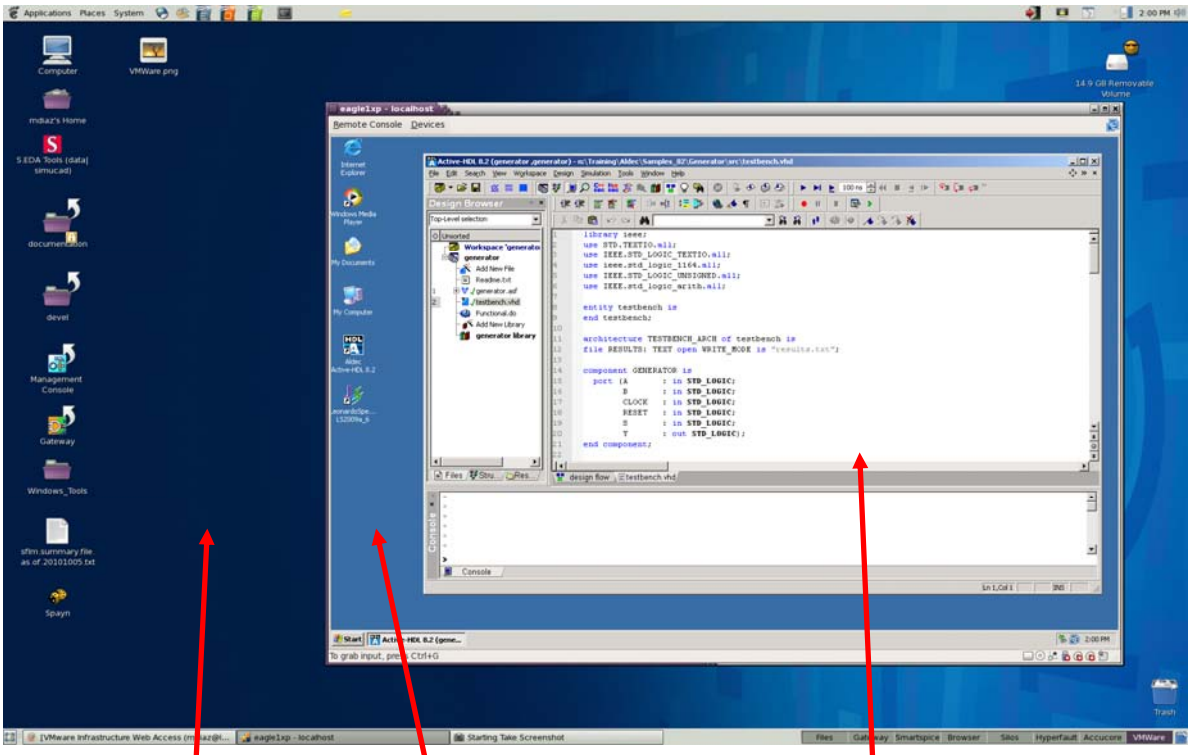


Figure 2.4 – Virtual Operating System

The backup software in the system was also tested for automatic backing-up procedures and fail-safe modes and guarantee recovery of files during power interruption or other event.

Detailed guides were created for Users and Administrators for use in the new system. These guides include the necessary steps for creating and administering user accounts, passwords, server service features and expanding the system with new workstations.

Conclusion

The configured Linux system adheres to the following criteria:

- Simple: improves overall reliability
- Standard: Uses proven technologies where ever possible.
- Documented: Concise recipes for installation and maintenance are maintained and preserved. They show detailed insight of the construction of the network.
- Reliable: Some components are redundant with focus on preservation of data. Minimization of system failure is achieved.

The system is capable of running any vendor's CAD tools and is ready for use in the Emulation design flow.

2b. Implementation of an improved CAD suite

Silvaco was chosen as the vendor provider for the design system's set of CAD tools. Silvaco offers the tools required to fully analyze a technology technical package, and generate optimal design and layout databases before fabrication. The transfer of files among these different tools does not require extra overhead to account for files being incompatible with another tool. One advantage of these set of tools is the ability to incorporate foundry process specific information from the creation of a new technology to a fully characterized logic cell library ready for design use.

The set of CAD tools from Silvaco was installed on the Linux system described in the last section. To complement the design flow and allow for the ability to target multiple design Hardware Description Languages (VHDL or Verilog), a couple of CAD tools from other vendors were integrated in the system using the installed virtual Windows environment. These tools provide additional capabilities without interfering with the established Silvaco CAD flow.

The set of CAD tools obtained can be divided into two major areas: Process Fabrication and IC design. The IC design tools were the target for the IBIF effort. The following is a brief explanation of the purpose of each of the design tools acquired:

Accucell: Tool used in the characterization of logic cells used in a specific technology library. This tool uses foundry specific information to generate models used throughout the digital design flow.

Gateway: Schematic editor tool that allows the creation of highly complex and hierarchical designs and allows seamless integration with simulator tools.

Smartspice: Provides accurate circuit simulation results for critical analog designs. It is used in conjunction with foundry device models.

Silos-X: Digital design simulator using Verilog as the default HDL language. It provides timing and functional analysis of designs.

CatalystDA: Converts Verilog digital netlists to Spice format netlists used in Layout-versus-Schematic (LVS) routines in the Expert tool.

Spider: Place-and-route tool that optimizes logic cell placement to minimize interconnection net lengths and clock-skew and delay management.

Expert: High performance hierarchical layout editor that allows netlist driven layout and is fully integrated with physical verification tools.

Guardian: Physical verification tool for LVS and Design-Rule-Check (DRC) routines.

Hipex: Parasitic extraction tool that identifies Resistance, Inductance, Capacitance (RLC) nodes that affect design performance.

ClarityRLC: Tool that performs reduction of RLC database for faster simulation analysis.

Accucore: Tool that provides Static Timing Analysis (STA) for a design before being released for fabrication. This tool identifies timing paths outside of the predefined target specification.

Hyperfault: Fault simulator that analyses the fault-coverage of vectors used in testing of the final IC products. This tool provides a metric for measuring the robustness of vectors used to detect fabrication imperfections in the final IC.

Additional tools that are not part of the Silvaco design suite, but contribute to the overall analysis of the design are:

Mentor Graphics Leonardo: Synthesis tool that uses Verilog or VHDL behavioral netlists to target specific technology logic cell libraries and generate Register-Transfer-Level (RTL) netlists for place-and-route.

Aldec Active-HDL: VHDL and Verilog netlist simulator that generates additional timing and debugging features for designs. This tool includes a code-coverage metric that detects untested areas of logic in the design using a testbench.

The token-based license scheme by Silvaco allows a pool of tokens to be shared among the many tools in the flow. As long as there are enough tokens to share among the tools at the same time, any tool can be used. Once, a specific task has been completed, the tokens for that tool go back to the common pool. In addition, all of the tools provided have the ability to be used in multi-core systems to expedite the execution of high complexity simulations. This allows for added flexibility during design surge events where time is of essence.

For the purposes of this contract, 100 tokens were acquired to support six personnel for training and use of these resources. Table 2.2 shows the amount of tokens required for running the tools mentioned previously.

CAD Tool	Tokens
Gateway	4
Smartspice	6
Smartspice Multicore	10
Expert	6
Expert Views	2
Guardian-DRC	10
Guardian-LVS	10
Guardian-NET	10
HIPEX	24
ClarityRLC	10
Spider	50
Accucell	24
Accucore	32
CatalystAD	18
SILOS-X	2
Hyperfault	20

Table 2.2 – Token Utilization per CAD tool

For additional tools running in the virtual Windows environment, the current file-based licenses were transferred over from the legacy design system. By doing this, the information generated by these tools will be backed-up by the management services already established in the Linux infrastructure.

Results

All of the tools in the Silvaco CAD flow were tested for flawless execution among the different computers in the system and communication with the main servers. Silvaco provides token management recording utilities that allow the examination of token usage and transfer among all users in the network. The token license scheme was tested for proper token distribution, check-in and check-out procedures. Multi-core execution of simulations was also tested. Figure 2.5 shows how all tokens were distributed for the period or performance for this contract.

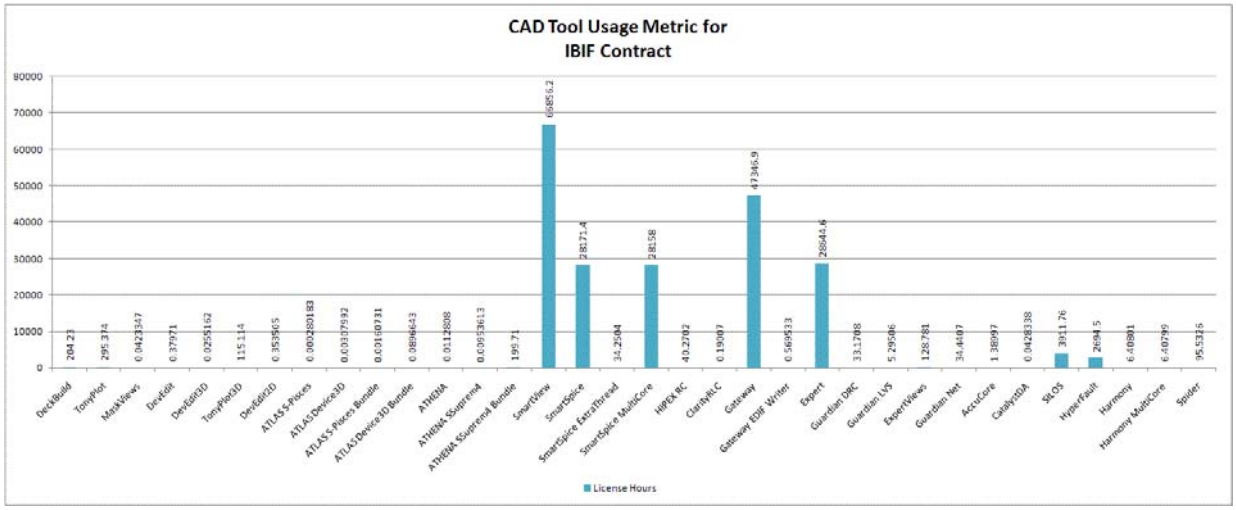


Figure 2.5 – Token Utilization for IBIF Contract

The tools in the Silvaco CAD suite were tested for correct execution in the system. It is anticipated that tools will be integrated into the design flow as needed. The tools shown in the figure with the highest usage rate, were utilized for executing the qualification task in this contract.

In addition, the visual rendering capabilities of the system were tested using a pre-configured layout database composed of 1 million transistors. Typically these large layout databases cannot load on the legacy design infrastructure. However, in the newly established system, this database loaded up in a few minutes and allows proper visual movement across the many layers of the layout database.

In the Emulation environment, one of the densest available technologies can reach up to 500,000 transistors. This system is capable of simulating upwards of 5 Million transistors as measured by Silvaco's proprietary benchmarks. The simulations take full advantage of a 64-bit Linux environment, multi-core processors and large memories.

Conclusion

The full suite of Silvaco CAD tools has been installed and tested successfully. They provide all of the capabilities for use in the Emulation design flow, and surpass all of the ones in the legacy system.

2c. Qualification of an improved design flow

Silvaco's set of tools are numerous and have many features. Design and layout users of the infrastructure had to be trained in each of these tools. Training sessions were organized with Silvaco's personnel where they took the design team through the steps in the design flow. Training was also done through use of ample documentation available with the tools and examples provided with the installations.

Some of the tools required customization for use with Sarnoff's specific foundry technology information. In the Emulation flow, sets of Gate-array structures had to be integrated into the system and optimized for efficient use. This is uncommon with normal industry practices where technology designs are fully customizable from the transistor level. In the case of the Emulation design flow, sets of gate arrays are pre-defined and customizable only at the via and metal levels where the different sets of placed logic cells are interconnected. This method allows for quick turn-around of final ICs from fabrication. In this effort, CMOS 0.8um set of arrays were transferred over from the legacy system. Tools were modified to address certain features required in the emulation flow. The transfer also involved the translation of technology files used in the verification stages of design and layout.

The first step in improving the accuracy of simulations to the actual results from tested ICs is the development of accurate characterization of logic cells. Silvaco's services were acquired to characterize the target library cells used for this task. This is a labor intensive process that requires interface with the foundry providing the target technology and the design team that will implement it. Silvaco's tool set provides all of the elements required for characterization when required. The characterized library files can be used to study the performance of individual cells and optimize the design accordingly. Figure 2.6 shows the compiled data for a single inverter in the digital library.

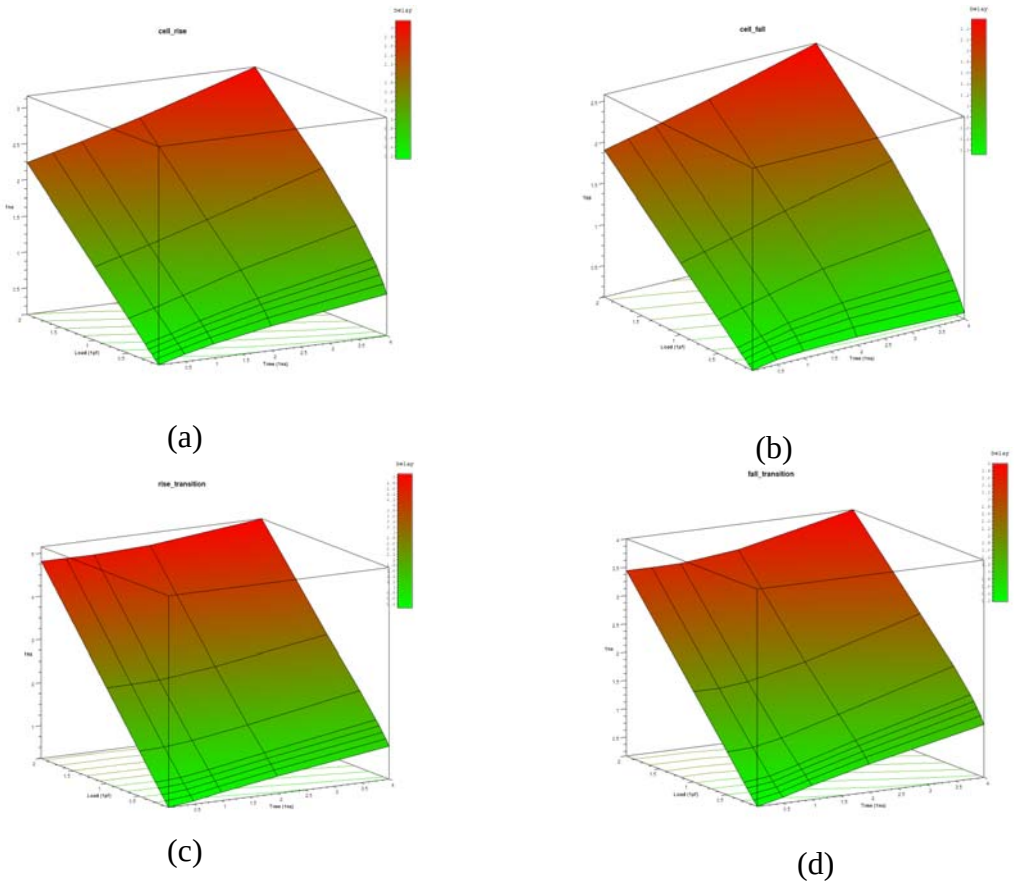


Figure 2.6 – Characterized information for an inverter cell: Slew vs. Load vs. (a) rise transition (b) fall transition (c) rise-time (d) fall-time

The characterization of cell libraries generates the files required for use in many of the tools in the design flow. This task uses the Accucell tool for the generation of these library files. Figure 2.7 shows how the information from the characterized cell library affects other tools in the design flow.

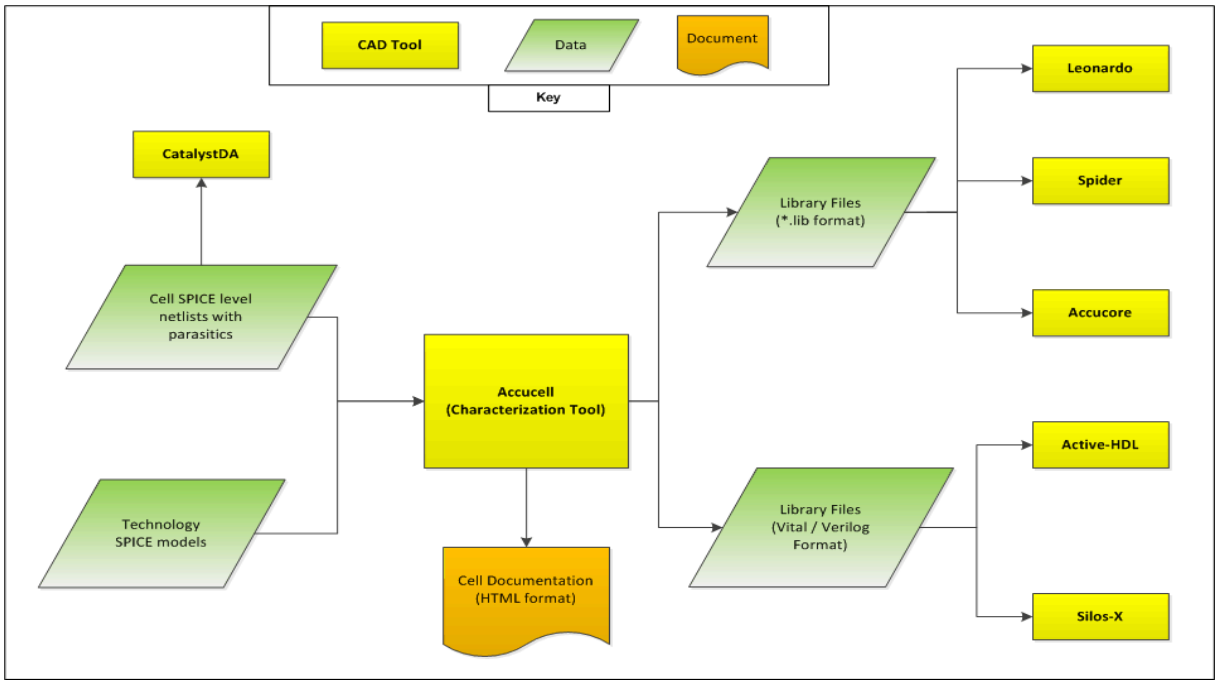


Figure 2.7 – Cell library characterization and implementation

For creating an optimal design flow, a known design was chosen for exercising the different elements in the CAD set of tools. This design referred as TST070 contains many of the issues encountered in complex designs. It contains the following:

- Synchronous and asynchronous paths
- Input, output and bi-directional cells
- Static and dynamic logic
- Buffered paths and delay cells
- Large amount of pins
- Targets the largest production array available at Sarnoff, the 200k CMOS 0.8um array.

Verilog and VHDL are the most common formats today for design and simulation of ICs. It is envisioned that with the Virtual environment capabilities in the system to run Windows based CAD tools, both VHDL and Verilog will be supported for designing ICs. This expands on the capabilities of this system to engage in additional emulation design challenges.

The original design information for TST070 created in the legacy design system is in VHDL format. For the purposes of this contract, the design had to be converted into Verilog format which is the standard language for the Silvaco tool set.

The Leonardo tool was used to generate a synthesized netlist that targets the characterized library mentioned previously. The generated netlist is in Verilog format. As is common with any CAD tool, setup scripts and files have to be created to use the tool in an effective manner. Figure 2.8 shows the Leonardo flow and the Graphical User Interface (GUI).

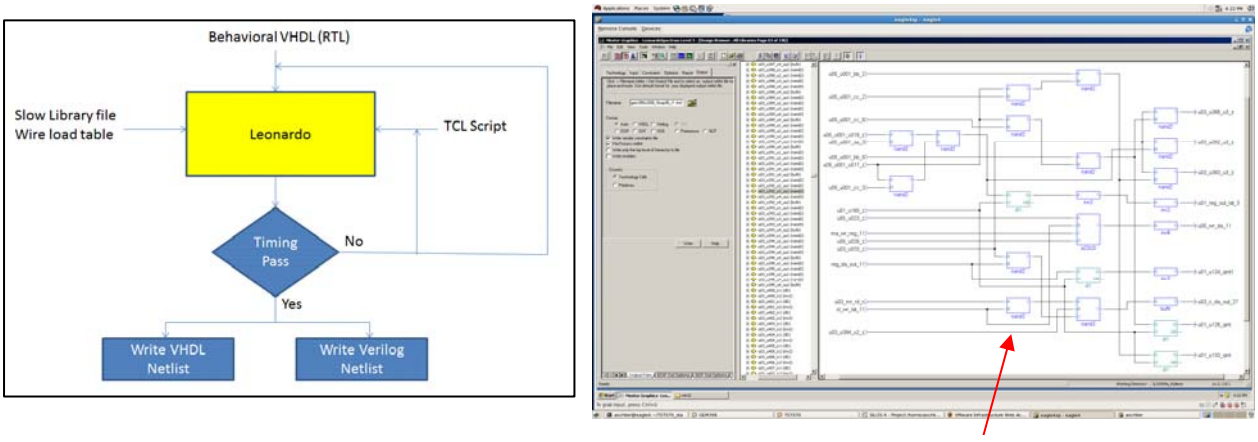


Figure 2.8 – Synthesis Flow (Leonardo)

For synthesized design validation in the Silvaco flow, Silos-X is used. The characterized cell library is loaded into the tool for functional and timing reference. A testbench is used to exercise the design with a set of pre-determined test vectors. If the functional testing does not meet the expected results, synthesis has to be re-started. Figure 2.9 shows the flow for the netlist validation using Silos-X and its corresponding GUI.

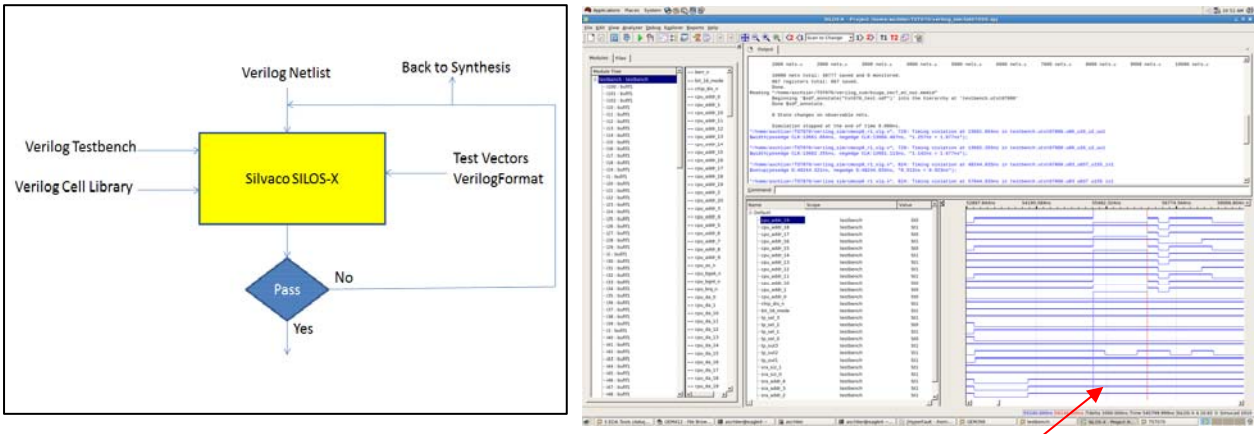


Figure 2.9 – Synthesized netlist validation using Silos-X

The validated netlist is then converted into a netlist format that is understood in the back-end design flow or layout. This format is used for expediting check routines by comparing two netlists as opposed to comparing two design databases. This approach greatly improves the time to validate the design artwork or layout. CatalystDA is used to convert the Verilog netlist, which describes cell level connectivity, into Spice format which describes transistor level connectivity.
Figure 2.10 shows the CatalystDA tool flow.

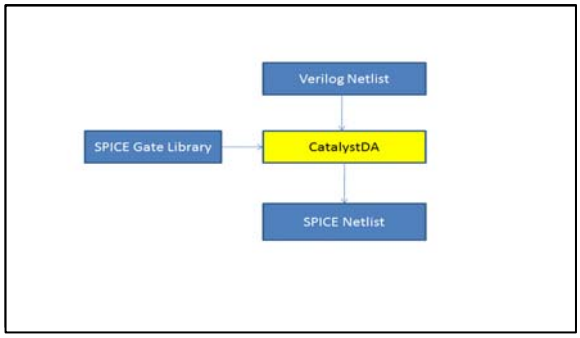


Figure 2.10 – CatalystDA tool flow

The Verilog netlist is used with the Place-and-Route tool to optimized placement of characterized library cells in a pre-defined transistor array. The Silvaco tool Spider was configured to use Sarnoff's gate arrays for this process. Spider uses technology information such as metal widths, resistance and capacitance to minimize the lengths of cell interconnections. The longer this interconnects are, the more delay is generated in the design affecting its performance. This is critical especially when clock nets need to meet a minimum skew delay. Cell fanout and buffering are also optimized. TST070 was place-and-routed to desired specifications using Spider.

Besides place-and-route, there are other layout features that are handled at later stages. The Spider generated database is loaded into the Expert layout tool for final optimization of IO cells and optimization of power distribution. This tool will generate the GDSII mask information for fabrication once all simulations and physical checks are completed.

Guardian is a verification tool that checks the integrity of the design netlist and the physical layout. As mentioned before, the Spice netlist generated from CatalystDA is used to run a LVS check against a Spice netlist generated from Expert. If the comparison succeeds, the DRC check is run to look for violations of physical design rules and unacceptable connections that can cause short or open failures in the final IC.

The last step in the layout flow is to extract all of the parasitics from the layout database and generate a Detailed Standard Parasitic Format (DSPF) file for simulation. This is accomplished by using the Hipex extraction tool. The resistance and capacitance from the final interconnections is extracted into a Spice

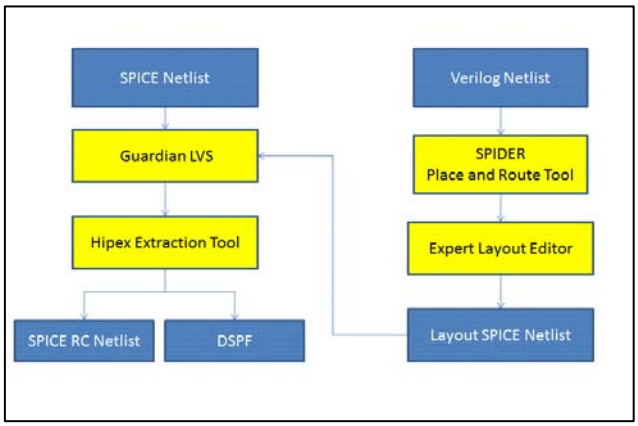


Figure 2.11 – Layout flow

file and a DSPF file. These files are used for final simulations. Figure 2.11 shows the entire layout flow.

The final validation involves the analysis of design timing, functional behavior including path delays and the robustness of test vectors used to exercise the final product IC. Silvaco's Accucore tool is used to analyze the static timing paths (STA) of the design. The reports generated are compared to customer specifications for approval of physical layout. Figure 2.12 shows the Accucore flow.

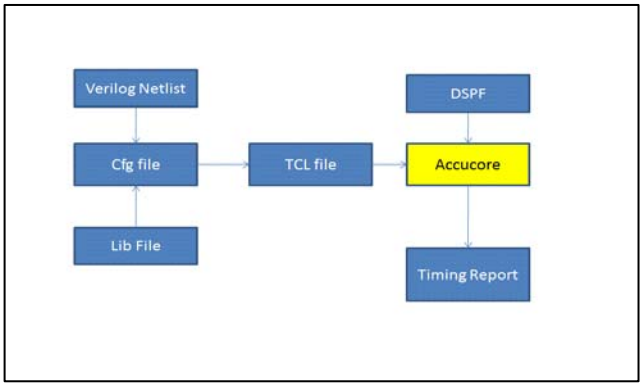


Figure 2.12 – Accucore flow

For the final functional simulation, using the DSPF file generated previously, a SDF file is created to use with the Silos-X tool. The final Verilog netlist is loaded and it's exercised with accurate timing information contained in the SDF file. The characterized cell library is used for the functional behavior of the cells. Timing performance not observed during the STA analysis is studied in this step. This is also known as back-annotation simulation. Each of these final reports increases the chances of success for the production IC. Figure 2.13 shows the final Silos-X flow.

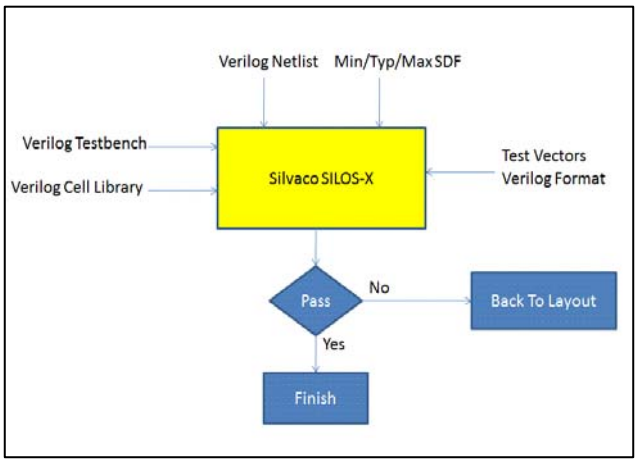


Figure 2.13 – Back-annotation flow

The last step in the design flow is to generate fault coverage metrics for the vectors to be used in testing. The robustness of the test vectors is measured in a percentage formula which describes the amount of failures or faults to check versus the amount of failures or faults being checked. The higher the percentage value, the less probable that a faulty product is release undetected. The reports generated at this step help in improving the overall quality of the product IC. Figure 2.14 shows the fault analysis flow.

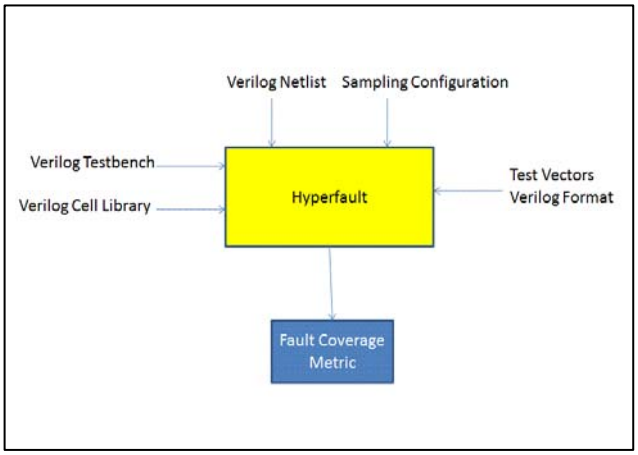
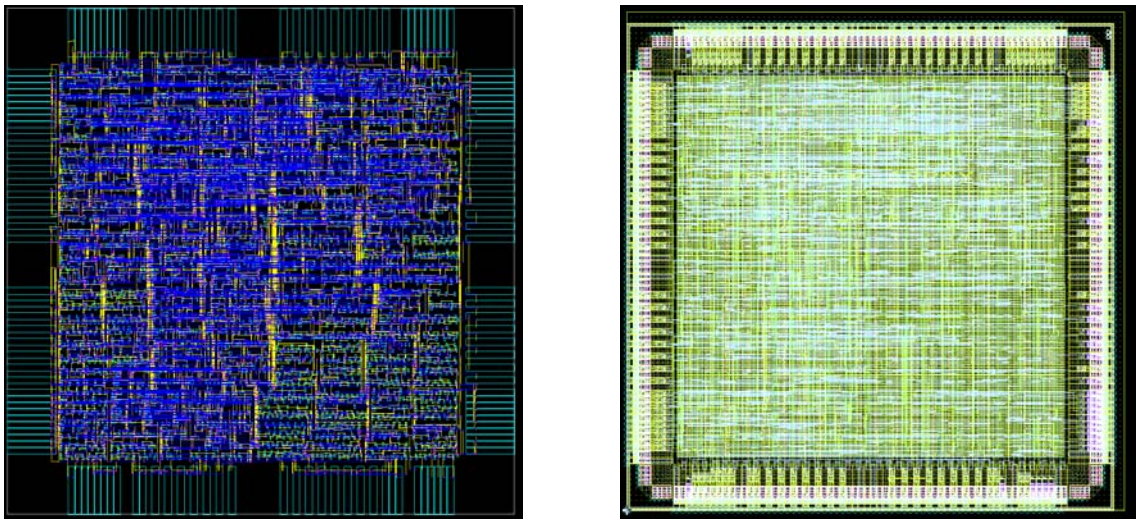


Figure 2.14 – Fault Analysis Flow

During the entire design flow there are many checks and balances to conserve the integrity of the design and measure its performance. If the design does not meet any of the criteria, more design cycles may be required before a final design is released. The ability to transfer information from one tool to another without translation or compatible file issues greatly improves the time involved to go through these iterations. Silvaco's suite allows the seamless transfer of information across all of its CAD tools.

Results

The design TST070 was exercised through the Silvaco flow and reports were generated at each of the stages. Several tool customizations were implemented due to the specific needs of the Sarnoff foundry and flexibility to handle gate-arrays. All of the steps in the design flow were completed successfully and where issues were encountered, support from Silvaco was crucial for resolution. Figure 2.15 shows the TST070 place-and-route database and the final GDSII as observed from the Expert tool. The GDSII is used to generate the production masks for this design.



(a) (b)

Figure 2.15 – TST070 layout database (a) Place-and-Route (Spider) (b) GDSII (Expert)

The final TST070 design was examined in the Hyperfault tool and test vector fault coverage was analyzed. Using existing test vectors the fault detection rate was measured to be 71%. This shows there's room for improvement for the test vectors used. Ideally the designer will target the fault metric as close to 100% as possible. The report shows the number of faults detected and

method applied. Figure 2.16 shows Hyperfault's Graphical Unit Interface and corresponding fault histogram showing activity per vector line.

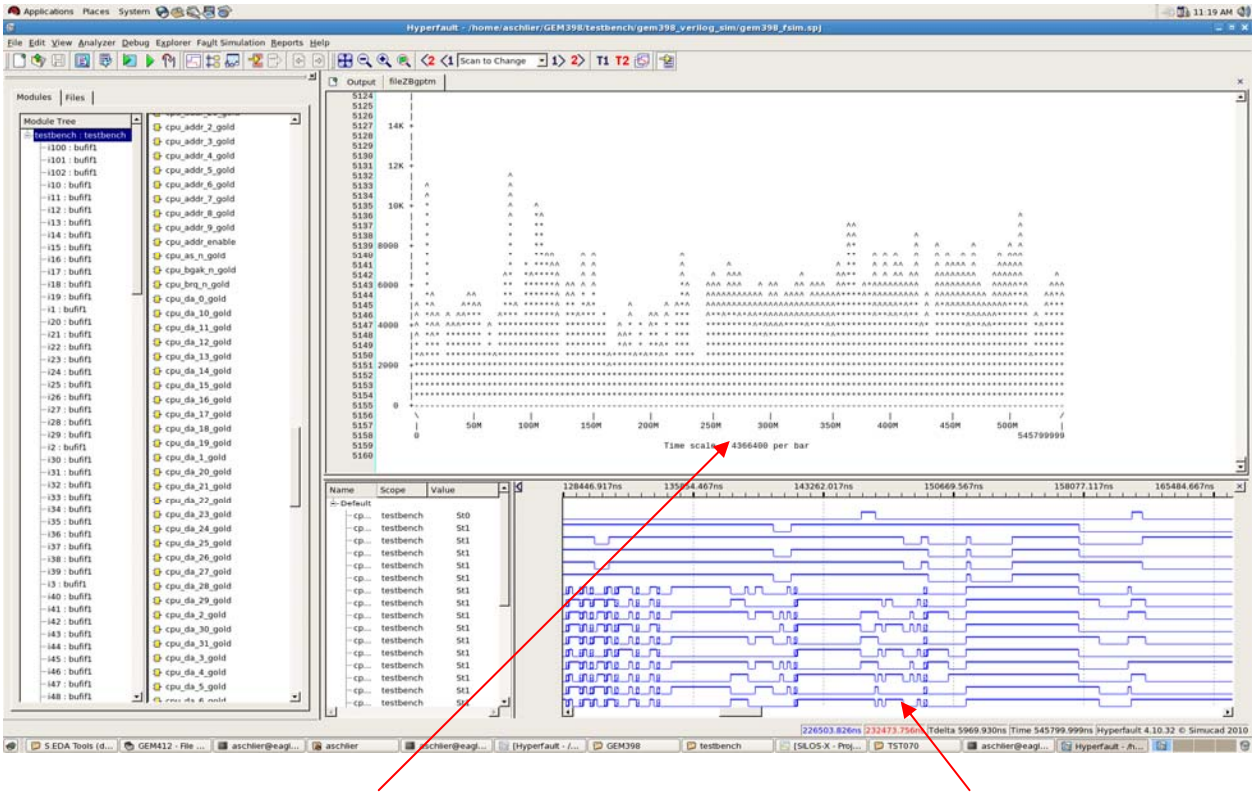


Figure 2.16 – Fault Analysis using Hyperfault

A summary of the fault report showing the fault coverage metric is shown in table 2.3.

	Number Faulted		Hard Detection		Possible Detection		Hypertrophic Detection		Undetected Faults	
	Count	%	Count	%	Count	%	Count	%	Count	%
.SLOW	38	10	23	61	1	3	4	11	10	26
.SHIGH	38	10	27	71	3	8	5	13	3	8
.ISLOW	840	10	458	55	30	4	90	11	262	31
.ISHIGH	835	10	489	59	18	2	93	11	235	28
TOTAL	1751	100	997	57	52	3	192	11	510	29
Actual Fault Detection Rate: 71% = 1241/1751										

Table 2.3 – Fault Analysis summary

The timing information gathered from Static Timing Analysis and final netlist simulation was compared to the measured results obtained previously for this known design. Table 2.4 shows this comparison and the level of accuracy.

Timing Path	Propagation Delay (ns)			% Difference	
	Silos-X	Accucore STA	Measured	Silos-X	Accucore STA
TPLH7	17.2	13.6	14.5	18.62	6.21
TPHL6	13.7	13.5	10.55	29.86	27.96
TPLH6	15.3	13.4	11.8	29.66	13.56
TPLH4	15.3	13.6	11.99	27.61	13.43
TPHL8	10.1	8.5	10.3	1.94	17.48
TPHL10	9.35	7.7	9.3	0.54	17.20
TPHL17	13.1	10.7	10.6	23.58	0.94
TPLH18	20.5	21.7	18.8	9.04	15.43
TPLH19	19.4	20.4	21.3	8.92	4.23
			Average	16.64	12.94

Table 2.4 – Comparison of simulation versus measured

As observed in table 2.4, different paths have different levels of accuracy when compared to results obtained from Silos-X or Accucore. The difference between simulation and measured data includes variations in process manufacturing that could be as high as 10%. The final average result of 12.94% for STA simulation represents an improvement of 1.5X the accuracy results obtained before the implementation of the system. Small adjustments to characterized libraries can represent larger accuracy improvements.

The design cycle time for TST070 using the Silvaco CAD toolset was measured to be 1,872 processor hours. This number was calculated using Silvaco's token management feature where each tool is measured by token-hours times a multiplier. The token multiplier for each tool is shown in table 2.2. Figure 2.17 shows the relative utilization of tools for the TST070 design cycle.

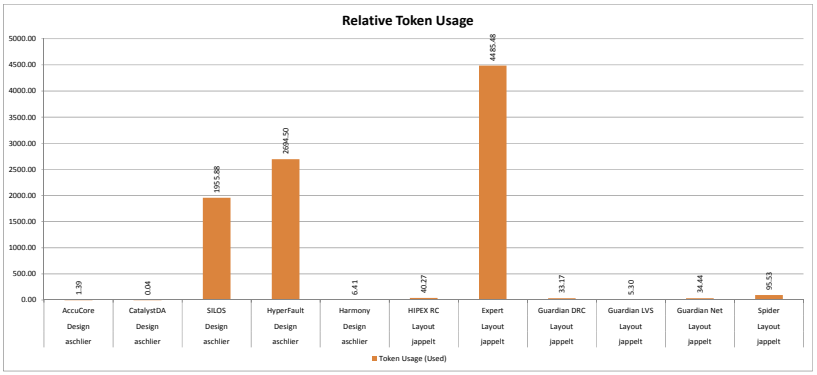


Figure 2.17 – Relative tool utilization for TST070

The overall design cycle time for TST070 is calculated to be around 2.60 months representing an improvement of more than 50% the time spent for the same design in the legacy system.

The finalized design flow is shown in figure 2.18. The figure shows an overall overview of the steps taken with the corresponding Silvaco tool being used in that particular step. The improved system provides the capability of a design flow utilizing one CAD tool vendor, and one Operational System based on a Verilog design. Tools from other vendors are integrated to extend the ability to target VHDL based designs. Even though there are many steps involved, the uninterrupted flow of information across the design flow is paramount for delivering good quality products on time.

The Silvaco tool-suite added features to the design flow that did not exist in the legacy system. These additional steps provide invaluable data for ensuring compliant finalized product ICs. The design flow is flexible to accommodate surge demands through a robust token-license system and ability to run multiple processors for complex simulations.

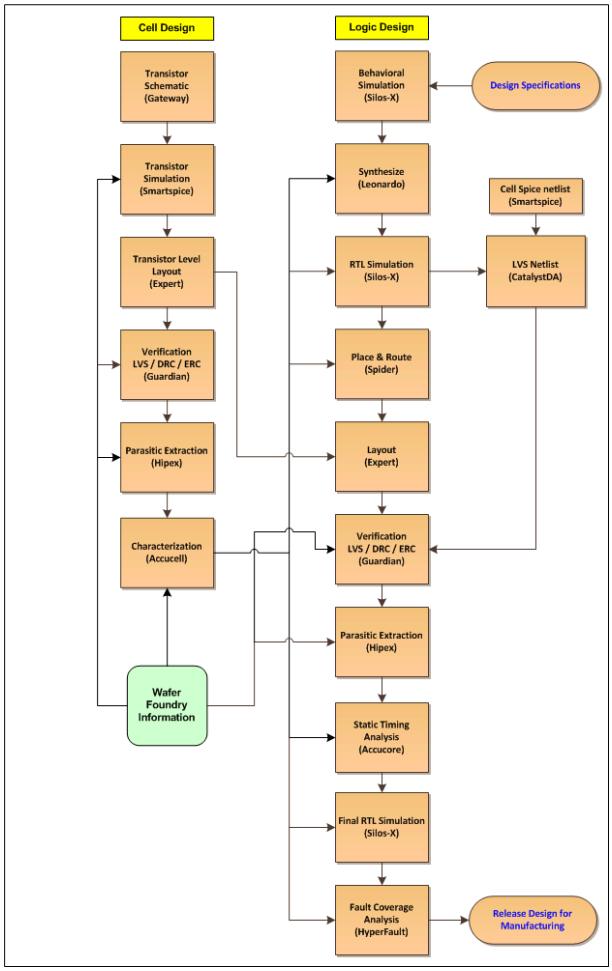


Figure 2.18 – Final Design Flow

Conclusion

Manufacturing technology improvements to the emulation design capability provide the following design process improvements:

- Isolation from internet, enhanced security
- Capability to target designs well beyond 500,000 gates
- Single Operational System
- Single CAD tool provider
- Token license flexibility
- Capability to indefinitely preserve the legacy design database including more than 400 designs currently in production and in use in various military platforms.

These overall benefits significantly assists the ability of DLA's emulation programs to support any effort for critical IC's necessary to supply and support Warfighter equipment.